



## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application #6

Applicant(s): Stephen V. Kosonocky  
Docket No.: YO999-369  
Serial No.: 09/589,716  
Filing Date: June 8, 2000  
Group: 2124  
Examiner: Chat C. Do

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: Lisa L. Tulpio Date: June 25, 2003

Title: Dynamic Adder with Reduced Logic

INFORMATION DISCLOSURE STATEMENT

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Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

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Technology Center 2100

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicant's attorney wishes to bring to the attention of the Patent and Trademark Office the following document listed on the accompanying Form PTO-1449: R.P. Brent et al., "A Regular Layout for Parallel Adders," IEEE Transactions on Computers, Vol. C-31, No. 3, p. 1-9, March 1982. A copy of the listed document is enclosed.

Please charge the amount of \$180 in accordance with 37 C.F.R. §1.17(p) to **International Business Machines Corporation Deposit Account No. 50-0510**. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0510** as required to correct the error.

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability, or as a representation that no other material information exists.

Respectfully submitted,

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Date: June 25, 2003